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A Power Silicon Microwave MOS Transistor

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Abstract—**Vertical MOS silicon power transistors for microwave power applications have been fabricated using an angle evaporation technique to position the gate electrode on the side of a mesa. These devices have produced 3-W output power at 1.5 GHz as a Class *B* amplifier and exhibit excellent linearity and noise properties. Device modeling has shown that parasitic capacitances are the chief factor limiting the frequency response, and the prospects for useful devices at 4 GHz are good.**

I. Introduction

THE frequency of operation of silicon MOS transistors has been extended to microwave frequencies in the past few years through the use of fairly sophisticated ion-implantation [1] and diffusion [2], [3] technologies. With these technologies, gate lengths on the order of 1 μm were achieved in small-signal transistor devices which demonstrated useful power gains in the 1–4-GHz frequency range. The extension of the implantation and diffusion (D-MOST) technologies to the development of large gate periphery, short channel devices for microwave power applications has not been reported to date.

Recently, a third technology (VMOST) was reported [4] which promised the processing of large periphery microwave MOST devices with high yield. Class *A* output power levels of up to 1.5 W at 0.7 GHz were obtained from a transistor cell having a total gate periphery of 0.62 cm. The VMOST structure has a mesa-type geometry, as shown in Fig. 1, which is formed by isotropic chemical etching.

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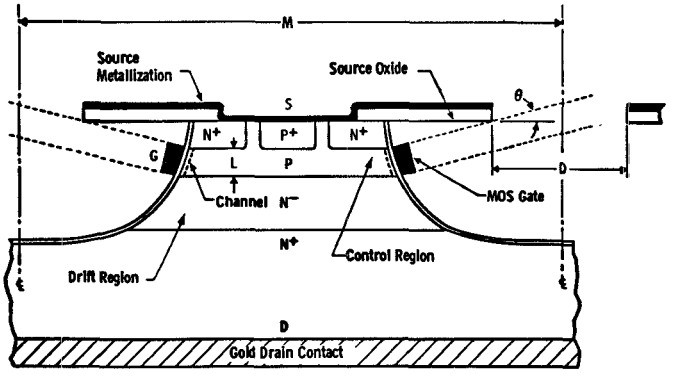

Fig. 1. Topology of vertical power MOS transistor geometry.

The length of the vertical n-channels is controlled by epitaxial growth, and the metal gate length by an angular metal deposition. This technology, referred to from now onwards as the ©VMOST technology, is distinctly different from the *V*-groove process [5] which uses a hydrazine anisotropic etch to form *V*-grooves. The gate in the *V*-groove transistor completely covers the oxidized etched surface, thereby giving rise to excess parasitic gate-drain capacitance which is detrimental to high frequency performance.

This paper will attempt to bring up to date progress which has been made in improving the power and frequency performance of the VMOST device. Descriptions of the latest device design and fabrication procedures are given in the next two sections. The microwave performance of some typical devices is shown in Section IV, while in Section V computer modeling results of the transistor are presented.

II. Device Design

Since its conception, the VMOST geometry has undergone a number of changes with attempts to solve the problems that limited the frequency response of the initial transistor [4]. These problems are common to all field-effect transistor designs, and are associated with 1) excess parasitic capacitance between the gate and drain terminals, 2) excessive parasitic capacitance between the gate and source terminals, 3) excess parasitic resistance in the source terminal, and 4) excess parasitic resistance in the gate terminal. Without these parasitics, the intrinsic VMOST device has a maximum cutoff frequency (f_{max}) in excess of 20 GHz, according to computer simulation of measured device parameters. In reality, the problem is one of keeping these excess parasitic elements to a minimum. To this end, a considerable portion of the time expended in the optimization process was used to redesign the transistor geometry and tighten up device fabrication tolerances.

A. Device Geometry

The geometry which is described in this paper is called the Mark IV design. A photograph of a finished Mark IV device is shown in Fig. 2. The transistor active area is 0.72 by 0.6 mm, and the chip area after dicing is 1 by 0.9 mm. As shown in Fig. 2, two main gate mesa contacts in the middle of the central gate bus connect the 68 gates of the 34 active transistor fingers. The total width of the 68 gates is 1.3 cm compared to 0.62 cm for the geometry described in [4]. The device is surrounded by isolation notches which interrupt the continuity of the gate metal around the periphery of the device and isolate the transistor gate metal from the outer periphery parasitic gate metal. Two parasitic gate mesa pads on each side of the transistor allow the parasitic gate metal to be grounded when necessary. The two source buses are tapered and each is designed to maintain a constant current density at any cross section along the bus.

One of the more interesting features of the VMOST technology is the manner in which all the 68 vertical gates are simultaneously connected together to the common gate bus and gate mesa bonding pads. The connection scheme is illustrated in Fig. 3. In this end view of two adjacent transistor fingers, it can be seen that during the angle evaporation of the gate electrodes, metal is also deposited in the trough region running perpendicular to the fingers. At the end of each finger, the metal gates widen and join together with the trough bus metal around the base of the mesa. The oxide overhang of each finger is also rounded at this end to minimize the discontinuity in the gate in going from the narrow to the wide bus region.

B. Impurity Concentration

The impurity concentration profile of the VMOST transistor is sketched in Fig. 1. The short p-channel layer (1 μm) was chosen to give the device a high unity current gain frequency f_T which under carrier velocity saturation

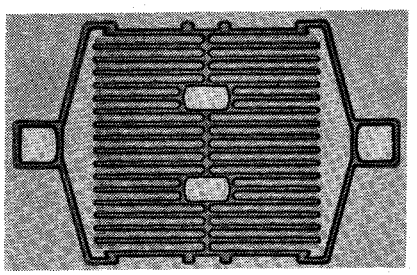

Fig. 2. Mark IV geometry, 1.3-cm gate periphery.

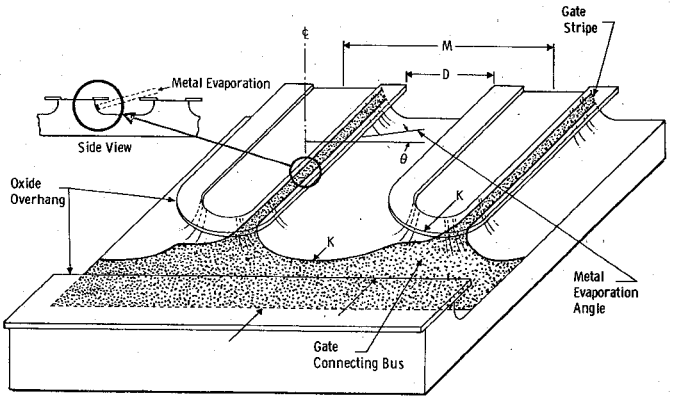

Fig. 3. Ghost view of fabrication of VMOST gate and gate interconnection bus using slant evaporation (only one side shown evaporated).

condition is determined by

$$f_T = \frac{V_s}{2\pi L_g} = 9.55 \text{ GHz} \quad (1)$$

assuming $V_s = 6 \times 10^6$ cm/s. This value of V_s appears to be more appropriate [1], [2] for MOS devices than the bulk value of 10^7 cm/s. The f_T of the VMOST transistor with 1-μm gate length is therefore nearly 10 GHz.

The concentration and thickness of the p-region determine the threshold gate voltage V_T and the punch-through drain voltage V_{PT}. If the concentration is too low (N_A comparable to N_D of the n^- drain drift region), depletion into the p-region occurs. If the p-region concentration is too high, the threshold voltage V_T required to turn the device "on" will be too large. For a p-region concentration of $N_A = 4 \times 10^{16}$ cm^{-3} and a 2-μm-thick drain drift region with $N_D = 10^{15}$ cm^{-3}, the depletion into the p-region is only 0.27 μm at a drain voltage of 30 V. The threshold voltage V_T, corresponding to this p concentration, can be calculated from (2)

$$V_T = \Phi_{ms} - \frac{Q_{ss}}{C_0} + 2\phi_f - \frac{Q_B}{C_0} \quad (2)$$

where Φ_{ms} is the potential difference between the conduction band edge of SiO_2 and the Fermi level of silicon: Q_{ss} is the surface charge density at the boundary of the Si–SiO_2 interface; ϕ_f is the Fermi potential; Q_B is the charge

induced in the surface depletion layer generated by the ionized donor atoms; and C_0 is the gate capacitance per unit area. If we assume an Al gate MOS structure as an example, with SiO_2 thickness of 10^{-5} cm ($C_0 = 35 \times 10^{-9}$ F/cm^2), p-type silicon with $N_A = 4 \times 10^{16}$ cm^{-3} ($\phi_f \sim +0.4$ V, $\Phi_{ms} \sim -1$ V), and $Q_{ss}/q = 5 \times 10^{11}$ cm^{-3}, then the threshold voltage at room temperature (300 K) is +1.7 V.

To enhance the drain voltage capability, an n^- drain drift region of approximately 2 μm is used in the VMOST structure. The concentration of this layer is sufficiently low ($\sim 10^{15}$ cm^{-3}) to ensure full depletion at a relatively small drain voltage (3–4 V). Under normal operation, the drain bias is considerably higher than this voltage, and the carrier velocity is saturated throughout the depletion region. At the same time, the length of this region is sufficiently short (< 2 μm) that transit time effects can be neglected. The transit time τ_t is approximately 33 ps, which corresponds to a phase delay of the short circuit drain current with respect to the gate voltage of 5.7° at a frequency of 1 GHz. This delay is sufficiently small as to be negligible except at extremely high frequencies (> 10 GHz).

In addition to drain voltage enhancement, the drift region increases the output impedance of the transistor and decreases gate-drain feedback due to any overlap of the gate electrode in the drain region.

The thickness of the n^- drift region is also governed by fabrication, since the thicker this region becomes the deeper will be the etched troughs, and the longer the oxide overhangs. While this problem is not fundamental, it nevertheless affects the density of devices in a given wafer.

III. Device Fabrication

The VMOST fabrication process is basically a four mask process, in which no critical photolithographic alignments below 3 μm are required. The first mask is used to leave p^+ grounding islands after the n^+ source diffusion, and the second mask defines the SiO_2 pattern for silicon etching to form the transistor fingers and bonding pads. The remaining two masks delineate the Si_3N_4 coverings for the source windows and the bonding pad ledges for metallization. The processing steps are illustrated in Fig. 4.

In step 1, the source n^+ regions are formed, followed by the p^+ grounding islands, step 2. The main transistor pattern is defined in step 3, after which the mesa fingers are formed by isotropic silicon etching down to the common n^+ drain region, step 4. Following thermal oxidation, step 5, the transistor is now ready for gate and source metallization, step 6. This occurs during the same angle evaporation since metal is deposited not only over the p-region to form the gate electrodes, but all over the top surface (source) of the mesas. A three metal system (Cr–Ni–Au) is used during gate, source, and drain contact evaporations instead of aluminum, which is more commonly used in the industry for MOS devices. The main reason for this is that aluminum, when evaporated at a low angle of incidence

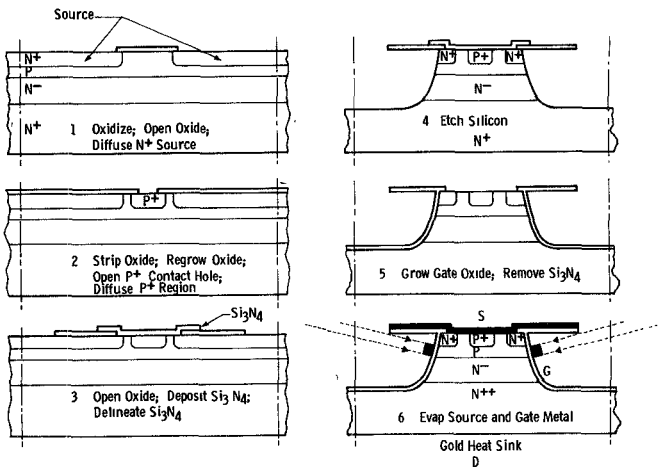

Fig. 4. Fabrication of VMOST.

to the substrate, is deposited as a dull "fibrous" film layer [6] with an electrical resistivity very much higher than the normal metal. The thicknesses of the various films on the gate are typically: Cr—600 Å; Ni—2000 Å; Au—6000 Å.

The angle of evaporation θ is determined by the position of the p-region and the source-oxide spacing D. Also, for a given spacing, the gate length will be $D \sin \theta$. In practically all the VMOST designs, an angle of approximately 15° is used, which gives an effective gate length of $0.26D$. This means that a 1-μm gate length can be achieved by using a relatively large D value of less than 4 μm. Since this is the minimum dimension on the VMOST structure, the photolithographic requirements are extremely nondemanding.

In a final processing step, the back substrate is thinned down to less than 25 μm to minimize thermal impedance and drain resistance, metallized, and gold plated to form gold heat sinks.

IV. Experimental Results

Fabricated VMOST devices have been characterized at low frequencies and at microwave frequencies by current-voltage, capacitance-voltage, and network analyzer measurements. Selected devices were also power tested as Class *A* or Class *B* common source amplifiers. From these data an accurate small-signal device model was developed to describe the high frequency performance and indicate those areas needing further development.

A. Low Frequency Measurements

The low frequency drain characteristics of a 1.3-cm periphery device, Run 28-3 series, are shown in Fig. 5. The maximum drain current exceeds 2 A and the gm is nearly constant at 200 mmho for drain currents over 400 mA. The turn-on resistance of this device, at a drain current of 1 A and a gate voltage of 16 V, is only 2 Ω, of which 1.5 Ω is due to the channel resistance. This leaves 0.5-Ω resistance for the total source and drain resistance losses. The maximum drain voltage of this device is 28 V.

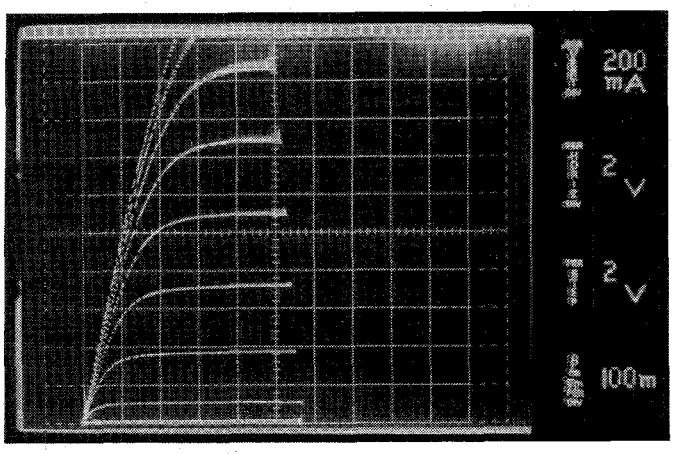

Fig. 5. Drain characteristics, Mark IV transistor.

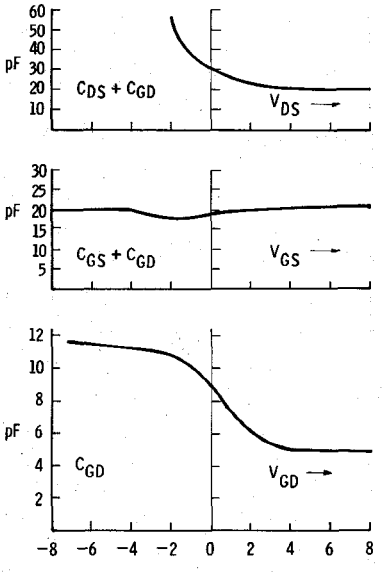

Fig. 6. Measured input, output, and feedback capacitances of VMOST 28-3-19.

The 1-MHz input, output, and feedback capacitance voltage variations of a typical VMOST 28-3-19 device are shown in Fig. 6. The output capacitance is composed of C_{DS}, a p-n junction capacitance, and C_{GD}, the gate-drain feedback capacitance. The input capacitance is the addition of C_{GS}, a MOS capacitance from gate to source, and C_{GD}. Ideally, this gate-drain feedback capacitance should be independent of voltage. The observed variation can be explained by assuming an overlap of gate metal above the n^- region of the device. This produces a MOS capacitor whose area varies with the drain source voltage, due to the depletion of the n^- region with the applied drain voltage. Calculations of the voltage dependence of C_{GD} based on gate overlap have shown good agreement with measured capacitance curves. The overlap of the gate metal can be attributed to the finite electron beam diameter of the *E*-beam evaporator used for the angle evaporation of the gate metal. From calculations using the evaporator physical dimensions, an extra 0.5 μm of gate length can result from the finite beam size. This effect is being minimized by a redesign of the evaporation facilities.

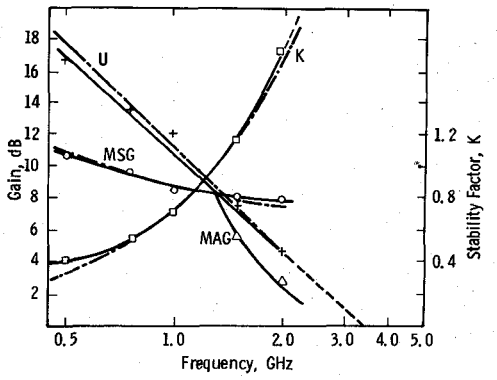

Fig. 7. Small-signal characteristics of 1.3-cm VMOST, 28-3-19, measured (——) and simulated (—·—).

B. High Frequency Measurements

The small-signal gain, stability and admittance parameters of VMOST, 28-3-19, are shown in Fig. 7. The extrapolated f_{max} of this device is 3.5 GHz and the maximum stable gain (MSG) is over 8 dB for frequencies up to 2 GHz. The maximum available gain (MAG) drops to 6 dB at 1.4 GHz. Smaller gate periphery devices (0.62 cm) have shown f_{max} values up to 4.5 GHz. The dashed lines in Fig. 7 represent the values predicted by the small-signal VMOST model which is described in Section V.

Power measurements on VMOST devices have been carried out under Class *A*, *AB*, and *B*, dc, and pulsed bias conditions. In all the microwave testing, the transistors were operated in the common source configuration on BeO chip carriers, with no internal matching networks. Tuning was achieved by a pair of coaxial slug tuners.

The power capability of VMOST 28-3-39 at 1 GHz is shown in Fig. 8. When biased Class *AB*, the output power was 2.8 W at the 1-dB compression point. The gain at this point is 5 dB and the power added efficiency is 21 percent.

Due to its relatively constant input and output capacitances and uniform transconductance, the VMOS transistor should exhibit lower distortion than bipolar or junction-gate field-effect transistors. To verify this, two-tone intermodulation distortion measurements have been carried out on a number of Run 28-3 series, 1.3-cm periphery VMOST devices operated under CW conditions. Due to high power dissipation and lower transconductance at the bias point used, the gain and output power were both reduced. Measurement of the intermodulation distortion under pulsed bias conditions, however, did not prove practical. Two signals 1 MHz apart were mixed through a 3-dB hybrid coupler and amplified by a TWT amplifier. The TWT output and the device output were observed on a spectrum analyzer. The results in Fig. 9 show the level of the third-order intermodulation product (IMP) in decibels below the output, plotted against the output power in

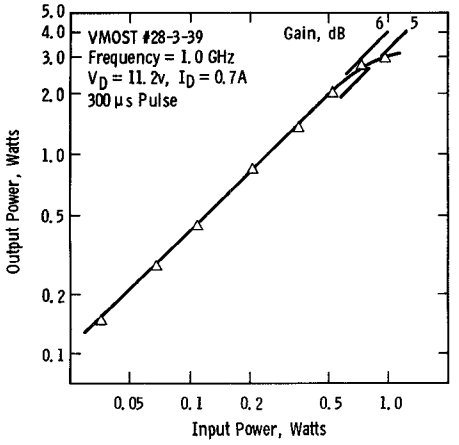

Fig. 8. Output power versus input power for VMOST 28-3-39 at 1.0 GHz. P_{out} is 2.8 W at −1-dB compression (5.2-dB gain).

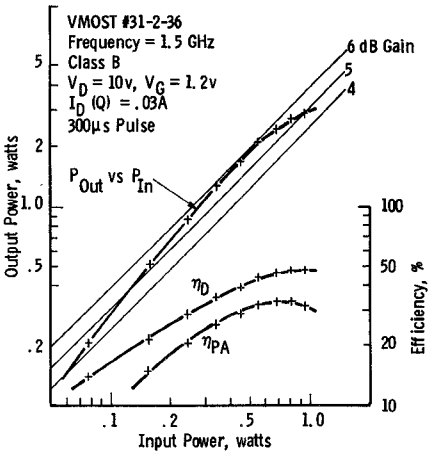

Fig. 10. Class *B* performance of 1.75-cm VMOST at 1.5 GHz.

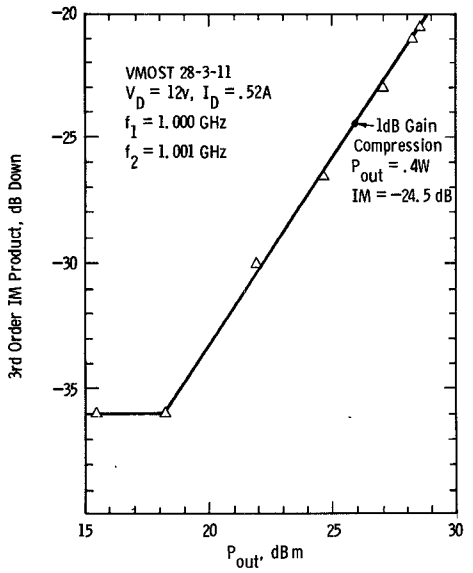

Fig. 9. IM product of VMOST versus output power.

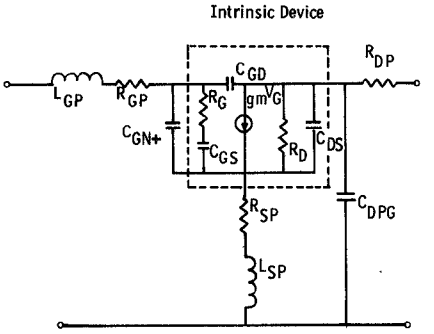

Fig. 11. VMOST model.

dBm. At low output power levels the IM product is a constant due to the contribution of the TWT amplifier. At the −1-dB gain compression point, the IMP level is still 24.5 dB below the output. The extrapolated 0-dB IM product intercept is 41.8 dBm. This IM product is lower than the reported values for bipolar devices.

The power capability of a larger periphery Mark V device at 1.5 GHz in Class *B* is shown in Fig. 10. At the −1-dB compression point with 4.8-dB gain, the output power is 3 W with 48-percent drain efficiency. The peak power-added efficiency is 33 percent at 2.5 W.

The noise figure of several Mark IV devices has been measured at 1 GHz using an AIL-type 75 Precision Automatic Noise Figure Indicator. The devices were dc biased for these tests at a drain current of 0.5 A. The measured noise figures were typically between 5.5 and 6 dB. Considering the large periphery (1.3 cm) of the devices, these values are extremely low and are comparable to the 4-dB noise figure at 1 GHz reported by Sigg *et al.* [2] for a 700-μm gate width D-MOS transistor. No attempts were made during the experiments to optimize the noise figure by varying the bias point.

V. Device Simulation

In optimizing the VMOST design, one of the most useful tools was a computer program which predicts device performance as each transistor parameter is altered. The equivalent circuit model for the VMOS transistor is shown in Fig. 11. In addition to the intrinsic device parameters, the model includes:

C_{GN+}	the gate-source overlap capacitance;
C_{DPG}	the output capacitance due to grounding parasitic device areas;
R_{SP}, R_{GP}, R_{DP}	the source, gate, and drain resistances, respectively, due to metallization and contact resistance losses;
L_{SP}, L_{GP}	the source and gate bond wire inductances.

Because the device is normally mounted on the output stripline of the chip carrier, the drain inductance is negligibly small.

Given the 13 model parameters, the program calculates the *y*-parameters, gains, and stability factor of the device

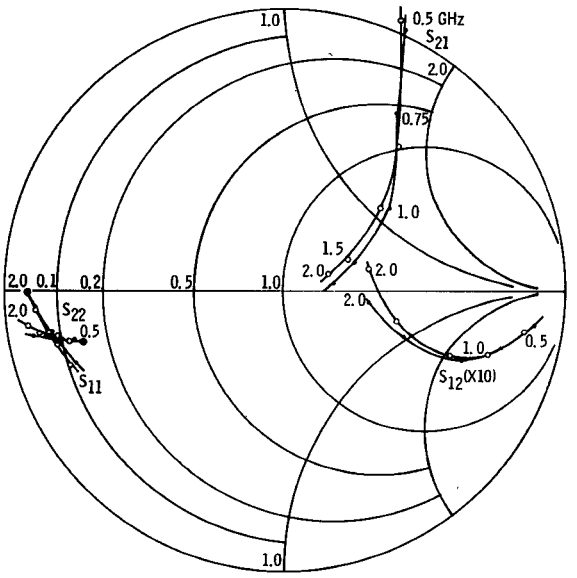

Fig. 12. Measured and calculated s parameters 1.32-cm VMOST 28-3-19. ●—measured. ○—calculated.

TABLE I
ELEMENT VALUES FOR VMOST 28-3-19

Element	Value
C_{GS}	5.13 pF
C_{GN+}	8.6 pF
C_{GD}	5.6 pF
C_{DS}	7.6 pF
C_{DPG}	5.0 pF
R_G	1.7 Ω
R_{GP}	0.5 Ω
R_{SP}	0.1 Ω
R_{DP}	0.1 Ω
R_D	40 Ω
g_m	0.21 mhos
L_{sp}	0.15 nH
L_{GP}	0.178 nH

over a specified range of frequencies. Included in the output are the unilateral gain, maximum stable gain, maximum available gain, and stability factor for the device, both with all the model elements and without the parasitic elements. This allows a direct observation of the effect of parasitic elements on the device performance.

Initial values for the device simulation are taken from the low frequency measurements and the network analyzer data. The g_m, drain resistance, R_D, and input, output, and feedback capacitances can be obtained from the low frequency data. The channel resistance R_G may be approximated as $1/(\lambda g_m)$, where λ is a value between 2.5 and 5 [7], [8]. From y parameters derived from microwave measurements these same parameters can be approximately derived along with some additional ones. The relations are:

$$B_{12} = -\omega C_{GD}$$

$$B_{11} = \omega[C_{GS} + C_{GD} + C_{GN+}]$$

$$B_{22} = \omega[C_{DS} + C_{DPG} + C_{GD}]$$

$$G_{21} = g_m$$

$$G_{11} = \omega^2[C_{GS}{}^2 R_G + (C_{GS} + C_{GN+} + C_{GD})^2 R_{GP}]$$

$$G_{22} = \omega^2(C_{GD} + C_{DS} + C_{DPG})^2 R_{DP} + 1/R_D.$$

These equations assume the source resistance is small and the frequency is low enough that the source and gate inductances have little effect. The values of L_{GP} and L_{SP} are estimated on the basis of the wire bond lengths between the device chip and its header.

The element values are adjusted by the computer to obtain a good fit to the measured y parameters. The match between measured and simulated device performance has been shown in Fig. 7 where the dotted lines show the simulated gain and stability factors for device 28-3-19, a Mark IV VMOST. In Fig. 12 the measured s parameters

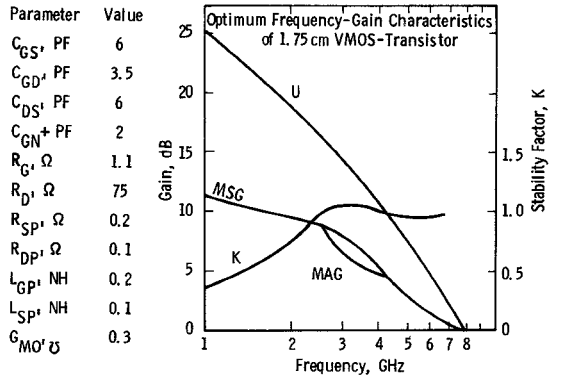

Fig. 13. Predicted performance of 1.75-cm VMOS transistor.

of this device can be compared to its model. The match for S_{11}, S_{22}, and S_{21} is very good while S_{12} deviates at the higher frequencies due to measurement inaccuracies. This occurs because the amplitude of S_{12} becomes very small (< -25 dB). The element values used for this model are listed in Table I.

This device model has helped identify several problem areas in the VMOST device during its development. In addition, it gives a reasonably accurate prediction of performance after each design perturbation, from which an extrapolated performance can be extracted. For example, a predicted performance of the latest Mark V device is shown in Fig. 13. This device would be usable up to 4 GHz with an available gain of 5 dB or more. Here the elements are realistic values which can be obtained once the fabrication steps have been perfected.

VI. CONCLUSION

The results that have been achieved by the VMOST device so far are encouraging, even at this stage of the development. Linear Class A or Class B power levels of up to 5 W appear to be feasible and within the reach of

present VMOST geometry. More important, the experiments also indicate that a microwave MOS transistor cell of extremely large periphery (up to 1.75 cm) can be fabricated to rival the unit cell power output of the microwave bipolar transistor. At the same time, the photo process requirements are relatively simple when compared with the bipolar process. Because of this, the yield of the VMOST process is high (up to 50 percent).

The current density and voltage capabilities achieved with present VMOS transistors are approximately the same as equivalent bipolar transistors. Other factors such as the absence of second breakdown phenomena and self-ballasting effects, should make the transistor even more attractive. These factors were quite evident during power testing of the VMOST devices.

Another important property which has been shown by the VMOST device is its linearity. The input and output capacitances and transconductance of the transistor are almost constant over a very large range of operating conditions. This, together with the high input impedance of the field-effect transistor, makes the device extremely attractive for broad-band linear power applications.

Some problems with material profile and gate metal overlap still remain to be optimized in the present fabrication process. These problems are not fundamental and should be solved in the near future. At that time, a 5-W silicon MOS transistor cell, capable of working at frequencies up to 4 GHz, will indeed have been realized.

The results achieved by the silicon VMOST to date show that the frequency capability of the device is inferior to present gallium arsenide MESFET devices of comparable gate length [9], [10]. This is to be expected since electrons in an n-channel GaAs MESFET will reach a higher effective drift velocity (1.5×10^7 cm/s) than their counterparts in a Si MOST because of surface scattering effects. In this respect, the VMOST device should not be compared to the GaAs MESFET as is often done mistakenly, but rather as a potential rival to the silicon bipolar transistor.

Acknowledgment

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